

## DESCRIPTION

## A SEMICONDUCTOR APPARATUS

5

TECHNICAL FIELD

The present invention generally relates to semiconductor apparatuses and especially relates to  
10 a semiconductor apparatus having a protection circuit for protecting the apparatus from electrostatic breakdown.

BACKGROUND ART

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Conventional semiconductor apparatuses are equipped with a protection circuit at the inner side of an input pad thereof, in order to prevent the semiconductor apparatuses from breaking down due to  
20 electrostatic current, as shown in Japanese Patent Laid-Open Publication No. 9-17954, for example.

Fig. 8 shows a circuit diagram of such a conventional semiconductor apparatus 1000 having a protection circuit. The semiconductor apparatus  
25 1000 is equipped with a protection circuit 50

between an input part (IN) 6 and semiconductor devices 10. The protection circuit 50 comprises a protection resistance 2 and a protection transistor 9 functioning as a diode.

5                   In the protection circuit 50, electrostatic electricity (charges) input at the input part (IN) flows through the protection resistance 2, resulting in reducing the electrostatic voltage and protecting internal  
10 semiconductor devices. In a case where the voltage input at the input part is very high and cannot be reduced enough by the protection resistance 2, the protection transistor 9 turns ON and allows the electrostatic charges to flow down to the ground Vss  
15 to protect the internal semiconductor devices 10. In this specification and claims, the protection transistor and devices in the semiconductor device side are collectively referred to as "internal circuitry".

20                   Fig. 9 is a cross-sectional view of the semiconductor apparatus 1000. An input pad 6 is formed integrally with a metal wiring layer (ME1) 5. A protection resistance 2 is formed by an N-well in a semiconductor substrate 1. In the N-well, a first  
25 electrode 3 of an N<sup>+</sup> region and a second electrode 4

of an  $N^+$  region are provided. The first electrode 3 is connected to the input pad 6 via the metal wiring layer (ME1) 5. The second electrode 4 is connected to a drain of a protection transistor 9 via another metal wiring layer (ME2) 7. A gate and a source of the protection transistor 9 are shorted and connected to ground  $V_{ss}$ . The semiconductor devices in the internal circuitry are connected to the metal wiring layer (ME2) 7.

10           In order to supply the semiconductor apparatus with electric power, a  $P^+$  region independently formed in the silicon substrate 1 is connected to ground  $V_{ss}$ , and an  $N^+$  region independently formed in the silicon substrate 1 is  
15 connected to a positive power supply  $V_{dd}$ .

The semiconductor apparatus 1000 is fully covered and insulated with an oxide layer 8, except an opening for the input pad 6. The metal wiring layer (ME1) 5 of the input pad 6 and the silicon  
20 substrate 1 are insulated with the silicon oxide layer 8.

As mentioned above, when high voltage static electricity is applied to the input pad 6, the electrostatic current normally flowing from the  
25 input pad 6 through the metal wiring layer (ME1) 5

and the protection resistance 2 to the metal wiring layer 7 (ME2), further flows through the drain and source of the protection transistor 9 to ground Vss. As a result, the internal semiconductor devices  
5 connected to the metal wiring layer (ME2) are not damaged.

There are other routes in which the electrostatic current flows from the first electrode 3 of the protection resistance 2, such as through  
10 the N-well region, to the positive power supply Vdd, or to ground Vss.

However, as shown in Fig. 10, in the conventional semiconductor apparatus 1000 the protection resistance 2 is placed between the input  
15 pad 6 and the internal circuitry 10. The first electrode 3 of the protection resistance 2 has substantially the same electrical potential as the input pad 6, and the first electrode 3 is formed in the silicon substrate 1; therefore electric  
20 discharge (leakage) occurs from the first electrode 3 to other circuitry formed in the silicon substrate 1, especially to semiconductor devices formed in the internal circuitry region 10, resulting in the breakdown of the semiconductor devices. In order to  
25 prevent such electric discharge, a length L2 between

the internal circuitry region 10 and the first electrode 3 needs to be increased, but that makes it difficult to miniaturize and highly integrate semiconductor devices.

5           As shown in Fig. 11, in a case where the input pad 6 is placed at a peripheral portion of the semiconductor apparatus 1100, especially adjacent to a corner, a length L3 between the internal circuitry region 10 and the first electrode 3 needs to be  
10 further increased, making it more difficult to miniaturize the semiconductor apparatus 1100.

#### DISCLOSURE OF THE INVENTION

15           It is a general object of the present invention to provide a semiconductor apparatus having a protection circuit, which can prevent electric discharge between an electrode of the protection circuit and other semiconductor devices  
20 and allow the miniaturization and integration of the apparatus.

          Features and advantages of the present invention are set forth in the description that follows, and in part will become apparent from the  
25 description and the accompanying drawings, or may be

learned by practice of the invention according to the teachings provided in the description. Objects as well as other features and advantages of the present invention will be realized and attained by  
5 the semiconductor apparatus particularly pointed out in the specification in such full, clear, concise, and exact terms as to enable a person having ordinary skill in the art to practice the invention.

To achieve these and other advantages and  
10 in accordance with the purpose of the invention, as embodied and broadly described herein, the invention provides as follows.

There is provided a semiconductor apparatus comprising a substrate with a pad, an  
15 internal circuitry region, and a protection resistance formed on the substrate;

the pad being connected to a first electrode of the protection resistance by wiring;

the internal circuitry region being  
20 connected to a second electrode of the protection resistance by wiring; and

the protection resistance protecting the internal circuitry region from electrostatic discharging;

25 wherein the pad is placed between the

protection resistance and the internal circuitry region.

In the semiconductor apparatus, the distance between the pad and the first electrode and  
5 the distance between the pad and the second electrode may be substantially the same.

There is provided a semiconductor apparatus comprising a substrate with a pad, an internal circuitry region, and a protection  
10 resistance formed on the substrate;

the pad being connected to a first electrode of the protection resistance by wiring;  
the internal circuitry region being connected to a second electrode of the protection  
15 resistance by wiring; and

the protection resistance protecting the internal circuitry region from electrostatic discharging;

wherein the distance between the first  
20 electrode and the internal circuitry region is greater than the distance between the second electrode and the internal circuitry region.

In the semiconductor apparatus, the  
25 substrate may be provided with a guard ring region

surrounding the pad, the internal circuitry region,  
and the protection resistance; and

distances from two sides of the first  
electrode, the first electrode being rectangular, to  
5 the guard ring region adjacent to the first  
electrode may be substantially equal.

The protection resistance may comprise a  
well region formed in the substrate; and

distances from the two sides of the first  
10 electrode to edge portions of the well region  
adjacent to the first electrode may be substantially  
equal.

Distances from two edge portions of the  
well region to the guard ring region adjacent to the  
15 well region may be substantially equal.

The pad may be placed on an insulating  
layer on the protection resistance.

The protection resistance may be formed by  
an impurity diffusion layer.

20 In the semiconductor apparatus, a  
protection circuit may be formed by the protection  
resistance and a protection transistor included in  
the internal circuitry region.



BRIEF DESCRIPTION OF THE DRAWINGS

Fig. 1 is a partial layout diagram of a semiconductor apparatus according to a first  
5 embodiment of the present invention;

Fig. 2 is a partial layout diagram of a semiconductor apparatus according to a second embodiment of the present invention;

Fig. 3 is a partial cross-sectional view  
10 of a semiconductor apparatus according to a third embodiment of the present invention;

Fig. 4 is a partial layout diagram of the semiconductor apparatus according to the third embodiment of the present invention;

15 Fig. 5 is a partial cross-sectional view of a semiconductor apparatus according to a fourth embodiment of the present invention;

Fig. 6 is a partial layout diagram of the semiconductor apparatus according to the fourth  
20 embodiment of the present invention;

Fig. 7 is a partial layout diagram of the semiconductor apparatus according to a fifth embodiment of the present invention;

Fig. 8 is a circuit diagram of a  
25 conventional semiconductor apparatus having a

protection circuit;

Fig. 9 is a partial cross-sectional view of the conventional semiconductor apparatus having the protection circuit of Fig. 8;

5 Fig. 10 is a partial layout diagram of the conventional semiconductor apparatus of Fig. 8; and

Fig. 11 is a partial layout diagram of another conventional semiconductor apparatus.

10 BEST MODE FOR CARRYING OUT THE INVENTION

In the following, embodiments of the present invention are described with reference to the accompanying drawings.

15 [First Embodiment]

Fig. 1 is a partial layout diagram of a semiconductor apparatus 100 according to a first embodiment of the present invention.

The semiconductor apparatus 100 includes a  
20 silicon substrate 1, an internal circuitry region 10 formed on the silicon substrate 1, and a peripheral device region 20 formed around the internal circuitry region 10. The peripheral device region 20 is surrounded by a guard ring region 30. The  
25 guard ring region 30 arranged around the chip is

formed by a diffusion layer and connected to a metal wiring layer mentioned below in order to obtain a substrate electric potential. Further, the guard ring region 30 plays a role of preventing the chip  
5 from suffering damage when dicing the chip.

The peripheral device region 20 is provided with a protection resistance (electrostatic discharge protection resistance) 2, which comprises an n-well formed in the p-type silicon substrate 1.  
10 The protection resistance 2 is provided a first electrode 3 of an  $n^+$  region and a second electrode 4 of an  $n^+$  region.

The first electrode 3 is connected to the input pad 6 via a metal wiring layer (ME1) 5. On  
15 the other hand, the second electrode 4 is connected via a metal wiring layer (ME2) 7 to the protection transistor and semiconductor devices formed in the internal circuitry region 10. This circuit structure is similar to that in the semiconductor  
20 apparatus 1000 shown in Fig. 8. The metal wiring layers 5, 7 and the input pad 6 are made of aluminum or poly-silicon, for example.

Similar to the semiconductor device 1000 shown in Fig. 9, a silicon oxide layer (not shown)  
25 is formed on the silicon substrate 1, and the metal

wiring layers 5, 7 and the input pad 6 are formed on the silicon oxide layer. Since a silicon oxide layer has extremely high insulating characteristics even if it is thin, high dielectric strength can be kept even when the input pad 6 becomes close to the internal circuitry region 10. Therefore, the length L1 between the input pad 6 and the internal circuitry region 10 can be less than the length L2 between the first electrode 3 and the internal circuitry region 10 shown in Fig. 10.

In the semiconductor apparatus 100 shown in Fig. 1, the input pad 6 is placed between the internal circuitry region 10 and the protection resistance 2. Because of this arrangement, the distance between the first electrode 3 of the protection resistance 2 and the internal circuitry region 10 can be kept long enough.

In the semiconductor apparatus 100, while keeping the distance between the first electrode 3 and the internal circuitry region 10 long, it is possible to shorten the distance L1 between the internal circuitry region 10 and the adjacent input pad 6 compared with the distance L2 between the internal circuitry region 10 and the first electrode 3 of the adjacent protection resistance 2 in the

conventional semiconductor apparatus 1000.

The layout according to the first embodiment of the present invention makes it possible to increase the area of the internal circuitry region 10 in a constant size semiconductor apparatus and enables high integration. But if the area of the internal circuitry region 10 is held constant, it is possible to miniaturize the semiconductor apparatus and reduce manufacturing cost.

[Second Embodiment]

Fig. 2 is a partial layout diagram of a semiconductor apparatus 200 according to a second embodiment of the present invention. In this embodiment, an input pad 6 is placed near a corner of the semiconductor apparatus 200. The same or similar reference numerals shown in Fig. 2 indicate parts that are the same as or similar to parts shown in Fig. 1.

As shown in Fig. 2, a protection resistance 2 is placed near a corner of the semiconductor apparatus 200. A first electrode 3 and a second electrode 4 of the protection resistance 2 are placed at substantially the same distance from one side of a guard ring region 30

surrounding a peripheral device region 20. In other words, the longitudinal axis of the protection resistance 2 is substantially parallel to the one side of the guard ring region 30.

5               The input pad 6 is placed at the other side of the protection resistance 2 from the one side of the guard ring region 30. One side of the input pad 6 is substantially parallel to an internal circuitry region 10, and the distance between them  
10 is L1, the same as that in the semiconductor apparatus 100 mentioned above.

              The first electrode 3 of the protection resistance 2 is connected to the input pad 6 by a metal wiring layer 5. The metal wiring layer 5 is  
15 placed perpendicular to the longitudinal axis of the protection resistance 2, and along one side of the guard ring region 30. On the other hand, the second electrode 4 of the protection resistance 2 is connected to the internal circuitry region 10 by a  
20 metal wiring layer 7. The metal wiring layer 7 is placed to extend from the longitudinal axis of the protection resistance 2 and along one side of the guard ring 30.

              As shown in Fig. 2, the rectangular first  
25 electrode 3 is arranged so that its two sides are

apart from the L-shaped guard ring region 30 by distances a and b, respectively. It is desired to make the distances a and b equal to each other. By making them equal, the distances between the guard  
5 ring regions 30 and the first electrode 3 are equal, and therefore the conditions of discharging from the first electrode 3 to the guard ring region 30 become uniform with respect to the two sides. As a result, there is no deviation in discharging characteristics,  
10 increasing the discharging resistance.

Especially in the semiconductor apparatus 200, since it is possible to make the side length of the first electrode 3 greater than in the semiconductor apparatus 100, it is possible to make  
15 the distances a, b between the first electrode 3 and the guard ring region 30 less than in the semiconductor apparatus 100.

In this manner, by adapting the layout according to the second embodiment of the present  
20 invention, the semiconductor apparatus 200 can be highly integrated and miniaturized.

In the semiconductor apparatus 200, the distance between the internal circuitry region 10 and the guard ring region 30 can be made less than  
25 in the semiconductor apparatus 100.

In the above embodiment, the longitudinal axis of the protection resistance 2 is parallel to one side of the guard ring region 30. The longitudinal axis can be oriented at any angle with respect to the one side of the guard ring region 30, as long as the distance between the first electrode 3 and the internal circuitry region 10 is greater than the distance between the second electrode 4 and the internal circuitry region 10.

10 In the above embodiment, the distances a, b from two sides of the first electrode 3 to the guard ring region 30 are set equal. Further, it is desired to also make the distances from two sides of the first electrode 3 to the edges of the well region forming the protection resistance 2 equal. 15 And it is also desired to make the distances from the edges of the well region to the guard ring region 30 equal.

This structure can avoid any deviation in the discharging characteristics and increase the discharging resistance.

[Third Embodiment]

Fig. 3 is a partial cross-sectional view of a semiconductor apparatus 300 according to a third embodiment of the present invention. Fig. 4 25



is a partial layout view of the semiconductor apparatus 300. The same or similar reference numerals shown in Fig. 4 indicate parts that are the same as or similar to parts shown in Fig. 1.

5                In the semiconductor apparatus 300, similar to the above semiconductor apparatus 100, a protection resistance 2 is formed in a silicon substrate 1, a second electrode 4 of a protection resistance 2 is connected to internal circuitry 10  
10 via a metal wiring layer 7. An input pad 6 is provided above the protection resistance 2, and connected to a first electrode 3 via a metal wiring layer (not shown). The distance between the input pad 6 and internal circuitry region 10 is L1, the  
15 same as in the first and second embodiments.

As shown in Fig. 3, the input pad 6 and the protection resistance 2 are insulated with a silicon oxide layer.

In Fig. 4, the protection resistance 2  
20 that is actually hidden by the input pad 6 is illustrated for easily understanding the layout.

In the layout according to the third embodiment of the present invention, the input pad 6 is provided above the protection resistance 2 and  
25 therefore it is possible to highly integrate and

miniaturize the semiconductor apparatus 300 while securing enough distance between the first electrode 3 and the internal circuitry region 10.

Especially overlapping the input pad 6 and the protection resistance 2 makes it possible to further miniaturize and highly integrate the semiconductor apparatus 300.

[Fourth Embodiment]

Fig. 5 is a partial cross-sectional view of a semiconductor apparatus 400 according to a fourth embodiment of the present invention. Fig. 6 is a partial layout diagram of the semiconductor apparatus 400. The same or similar reference numerals shown in Fig. 6 indicate parts that are the same as or similar to parts in Fig. 1. In Fig. 6, a protection resistance 2 that is actually hidden by an input pad 6 is illustrated for easily understanding the layout.

The semiconductor apparatus 400 has the same structure as the semiconductor apparatus 300 except that the protection resistance 2 is long (the distance between a first electrode 3 and a second electrode 4 is long) and extends out at both sides of the input pad 6. This structure is utilized when increasing a resistant value of the protection

resistance 2.

Also in the layout according to the fourth embodiment, it is possible to highly integrate and miniaturize the semiconductor apparatus 400 while  
5 securing enough distance between the first electrode 3 and an internal circuitry region 10.

[Fifth Embodiment]

Fig. 7 is a partial layout view of a semiconductor apparatus 500 according to a fifth  
10 embodiment of the present invention. The same or similar reference numerals shown in Fig. 7 indicate parts that are the same or similar to parts shown in Fig. 1. Also in Fig. 7, a protection resistance 2 that is actually hidden by an input pad 6 is  
15 illustrated for easily understanding the layout.

In the above semiconductor apparatus 400, the longitudinal axis (between the first electrode 3 and the second electrode 4) of the protection resistance 2 is substantially parallel to an edge of  
20 the internal circuitry region 10. In the semiconductor apparatus 500, the longitudinal axis of a protection resistance 2 is perpendicular to an edge of an internal circuitry region 10. Except for this structure, semiconductor apparatuses 400 and  
25 500 are substantially the same.

In this layout according to the fifth embodiment, by providing the input pad 6 above the protection resistance 2, it is possible to highly integrate and miniaturize the semiconductor apparatus 500 while securing enough distance between the first electrode 3 and the internal circuitry region 10.

Although input pads are utilized for explaining the present invention in the above embodiments, the present invention can be applied to output pads and other pads.

Instead of silicon substrates, other semiconductor substrates such as GaAs, etc., can be used. Further, instead of silicon oxide layers, nitrogen silicon layers, phosphor glass and other insulating materials can be used.

The present application is based on Japanese Priority Patent Application No. 2004-104136 filed on March 31, 2004, with the Japanese Patent Office, the entire contents of which are hereby incorporated by reference.